ABSTRACT OF THE DISCLOSURE

A RAM memory with a shared sense amplifier structure, in which sense amplifiers are arranged in strips between two adjacent cell blocks and are configured as differential amplifiers. In an exemplary embodiment, a one of four bit line pairs of the two adjacent cell blocks can be selected for connection to a sense amplifier at any one time using respective isolation transistor pairs, in response to a connection control signal fed to the latter. A signal sent on a word line coupled to a memory cell associated with the selected bit line pair, provides access to the memory cell by the sense amplifier.

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